PATENT ABSTRACTS OF JAPAN

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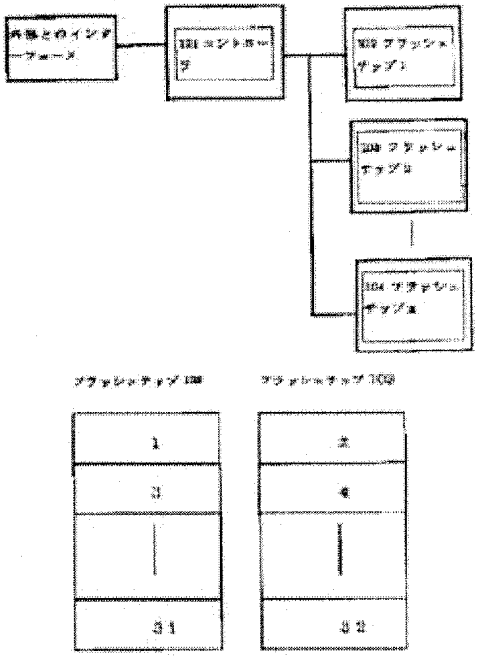
(54) STORAGE

(57)Abstract:
PROBLEM TO BE SOLVED: To improve the access speed by deciding whether the data should be interleaved according to the quantity of data to be written at a time and then writing the data in a flash memory.
SOLUTION: When the logical address of a storage and the information to be written are given from an external I/F, a controller 101 decides a specific area of a flash memory 102 where the data are actually written on an address conversion table existing at a part of the memory 102. The conversion table that is defined every 16 sectors (8448 bytes), for example, contains a bit to show whether the data should be interleaved. The controller 101 decides the said interleaving according to the quantity of data to be written at a time, sets a bit showing the interleaving in the conversion table if the interleaving is advantageous and writes the 1st and 2nd data in the flash memories 102 and 103 respectively. Thereafter, the data are alternately and continuously written in both memories 102 and 103 and accordingly the writing time is shortened.



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審査請求　未請求　請求項の数１　ＯＬ　（全　３　頁）

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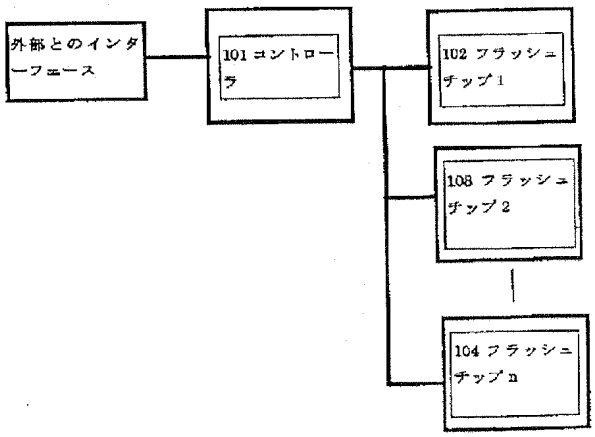
Ｆターム(参考)　5B060 HA02

(54)【発明の名称】　記憶装置

(57)【要約】
【課題】フラッシュメモリを使用した記憶装置のアクセス時間を短くすることにある。
【解決手段】フラッシュメモリを使用した記憶装置にデータを書き込む場合一度に書き込むデータ量に応じてインターリーブするかしないかを決定し書き込みを行う。



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【特許請求の範囲】

【請求項１】複数のフラッシュメモリチップとその制御を行うコントローラにより構成される記憶装置において概記憶装置に書込むデータをフラッシュメモリの連続したアドレスに書込むかあるいは複数のフラッシュメモリに交互に書込むかを決めるビットがありそのビットにしたがって書込み方法を切り替えることを特徴とする記憶装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はフラッシュメモリを使用した記憶装置に関するものである。

【０００２】

【従来の技術】複数のフラッシュメモリとその制御を行うコントローラにより構成される記憶装置ではそのデータの書き込みおよび読み出しをする場合にコントローラのシンリンダー、トラック、セクタにより構成される論理アドレスを変換テーブルによりコントローラがフラッシュメモリの物理アドレスに対応させていた。このコントローラがインターリーブという方法によりフラッシュメモリへの書き込み時間を短くしていた。インターリーブとは連続したデータを１つのフラッシュメモリの連続したアドレスに書き込むのではなく複数のメモリにまたがって書き込む方法である。たとえば10セクタのデータを書込む場合には、１セクタは512バイトとそのデータの管理情報16バイトの合計528バイトで構成されるので528×10バイトのデータをフラッシュメモリに書込む必要がある。フラッシュメモリに書込みを行う場合528バイトのデータをフラッシュメモリチップに転送しフラッシュメモリ内部のバッファに格納した後、フラッシュメモリに書込みコマンドを発行しフラッシュメモリにデータを書込む。フラッシュメモリチップにデータを転送するのに要する時間をtT、フラッシュメモリにデータを書込む時間をtWとすると10セクタ分のデータを１つのフラッシュメモリチップに書込むのに要する時間は１０×（ｔＴ＋tW）である。

【０００３】インターリーブでは10ある528バイト単位のデータのうち最初の528バイトデータをk番目のフラッシュメモリチップに書込み、次の528バイトデータをk+1番目のフラッシュメモリチップに書込み3番目の528バイトデータを再度k番目のフラッシュメモリに書込むという動作をする。

【０００４】このようにするとk番目のフラッシュメモリに528バイトデータの書込みが完了するまでの時間を待たずにk+1番目のフラッシュメモリチップにデータの転送を開始できる。したがって10セクタ分のデータを書込むのに要する時間は5×(tT+tW)+tTである。一般にtT<tWであるためインターリーブ動作をするとインターリーブをしない場合に比べて書込み時間が約半分になる。

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【０００５】

【発明が解決しようとする課題】しかしながら全ての書き込み動作に対してインターリーブを行うとかえって記憶装置としてアクセス時間を長くさせるという問題があった。たとえば記憶装置の中の１セクタのみのデータを書き換える動作を行う場合には528バイトのみのデータを書き換えれば良いはずである。しかしフラッシュメモリはたとえば528×16=8448バイトで構成されるブロックの単位で書き込みを行う。これは以下の理由による。フラッシュメモリは現在書込んであるデータに上書きをすることができず8448バイトの単位で一旦データを消去して書込みを行う。ある8448バイトのブロック内部の528バイトを書換える場合には8448のうち528バイトのみのイレーズすることはできないので従来格納されていた8448バイトのデータのうち528バイトのみ変更した8448バイトのデータを同じアドレス領域をイレーズした後再度書込むかあるいは他のイレーズ済みのエリアに書込む。いずれにしても8448バイト（528バイトを16回）の書込みが必要である。よってひとつのブロックの書込みを行う場合には16×（tT+tW）の時間を要する。これは１セクタのみ書換える場合でも複数セクタのデータを書換える場合でも同じ時間が必要である。

【０００６】たとえば2セクタのみの書込みが必要な場合にはインターリーブを行うと16×（tT+tW）＋tTの時間が必要であるがインターリーブを行わなければ16×（tT+tW）で書込みが終了する。一方16を超えるセクタの書込みを行う場合にはインターリーブした方が早くなる。17セクタの書込みを行う場合には２つの8448バイトのブロックの書込みを行う必要がある。インターリーブを行わないと一つ目のフラッシュメモリの16セクタのデータを書換えた後２つ目のフラッシュメモリの16セクタデータを書換える必要があるので2×16×(tT+tW)-tWの時間が必要である。しかしインターリーブを行うと16×(tT+tW)+tTで書込みができる。

【０００７】以上のようにインターリーブを行うことにより書込み時間が早くなる場合と遅くなる場合がある。

【０００８】

【課題を解決するための手段】本発明の記憶装置は、複数のフラッシュメモリチップとその制御を行うコントローラにより構成される記憶装置において概記憶装置に書込むデータをフラッシュメモリの連続したアドレスに書込むかあるいは複数のフラッシュメモリに交互に書込むかを決めるビットがありそのビットにしたがって書込み方法を切り替えることを特徴とする。

【０００９】

【発明の実施の形態】図１が本発明のブッロク図である。101はコントローラでありコントローラ101にはコントローラの処理を行うCPUとコントローラの処理プログラムを行うROMとCPUが一時的に必要なデータを保存するRAMとフラッシュメモリのデータの読み書きを行うため

のアドレス、データバスおよび記憶装置の外部とやりとりをするインターフェースから構成される。102, 103はフラッシュメモリでありコントローラ101によりアクセスされる。本実施例ではフラッシュメモリが２個の場合を説明しているがフラッシュメモリは２個以上ならいくつでも構わない。

【００１０】外部インタフェースからシリンダ、トラック、セクタという記憶装置の論理アドレスと書込む情報がコントローラ101に与えられるとコントローラ101はフラッシュメモリ102の一部にあるアドレス変換テーブルにより実際のフラッシュメモリのどのエリアにデータを書込むかを決定する。

【００１１】このアドレス変換テーブルを図２に示す。シリンダ、トラック、セクタがこのアドレス変換テーブルに入力されるとそれに対応したフラッシュメモリのアドレスが出力される。このアドレスにデータを書き込む。変換テーブルは16セクタ（8448バイト）毎に定義されている。このアドレス変換テーブルにはインターリーブするかどうかを示すビットがある。一度に書き込むデータ量によりインターリーブしたほうが有利かどうかをコントローラ101が判断し、有利なら変換テーブル内のインターリーブを示すビットをセットし、フラッシュメモリ102, 103にまたがりデータを書き込む。

【００１２】データを書き込む方法を図３に示す。フラッシュメモリは8448単位のブロックがいくつか含まれるがフラッシュメモリ102, 103の同時位置にあるブロックを使って図３のようにデータを書き込む。図３の数字がデータを書き込む順番を示す。１番目のデータをフラッシュメモリ102に書き込み、２番目のデータをフラッシュメモリ103に書き込む。以下同様に奇数番のデータをフラッシュメモリ102に偶数番のデータをフラッシュメモリ103に書き込む。このデータを読み出す場合にはアドレス変換テーブルのインターリーブを示すビットを読みフラッシュメモリ102と103から交互にデータを読み出す。もし一度に書き込むデータ量が少ない場合にはアドレス変換テーブルのインターリーブを示すビットをリセットし図４に示すように一つのフラッシュメモリに連続してデータを書き込む。このデータを読み出す場合にはアドレス変換テーブルのインターリーブを示すビットを参照し連続したデータを読み出す。

【００１３】

【発明の効果】以上のように１度に書き込むデータ量によりインターリーブをするかしないかを判断してフラッシュメモリに書き込むことによりアクセス速度を早くすることができる。

【図面の簡単な説明】

【図１】　本発明の１実施の形態を示すシステム構成図。

【図２】　アドレス変換テーブルの図。

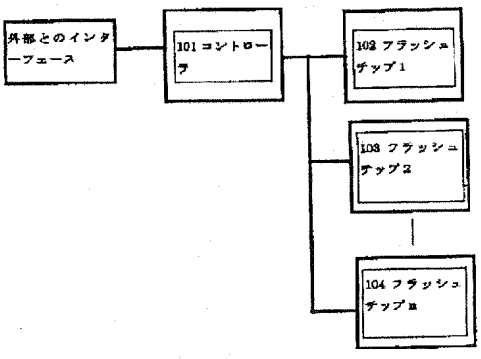
【図３】　インターリーブした場合のデータ書き込み例の図。

【図４】　インターリーブしない場合のデータ書き込み例の図。

【符号の説明】

101　コントローラ
102　フラッシュメモリ
103　フラッシュメモリ

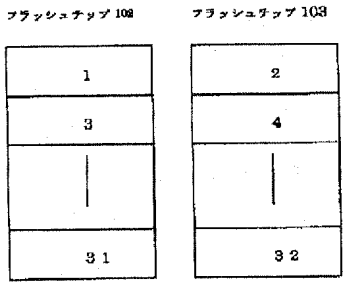
【図１】



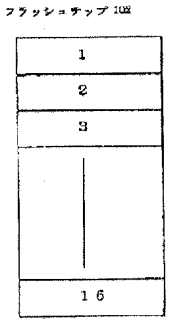
【図２】

シリンダ/トラック/セクタ	アドレス	インターリーブ
0/0/1～16	ブロックの先頭アドレス	y/n
0/0/17～31	ブロックの先頭アドレス	y/n
1/n/n～n+15	ブロックの先頭アドレス	y/n

【図３】



【図４】



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CLAIMS

[Claim(s)]
[Claim 1]By two or more flash memory chips and a controller which performs the control. Memory storage changing a method which there is a bit to decide and writes in whether data written in ********** in memory storage constituted is written in an address with which a flash memory continued, or it writes in two or more flash memories by turns according to the bit.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the memory storage which uses a flash memory.
[0002]
[Description of the Prior Art]When making writing and read-out of the data two or more flash memories with the memory storage constituted by the controller which performs the control, SHINRINDA of a controller, The controller was making the track and the logical address constituted by the sector correspond to the physical address of a flash memory with a translation table. This controller shortened writing time to the flash memory by the method of interleave. Interleave is a method which does not write continuous data in the address with which one flash memory continued, but is written in ranging over two or more memories. For example, to write in the data of ten sectors, since one sector comprises 512 bytes and a total of 528 bytes of 16 bytes of management information of the data, it needs to write 528x10 bytes of data in a flash memory. When writing in a flash memory, after transmitting 528 bytes of data to a flash memory

chip and storing in the buffer inside a flash memory, a write command is published to a flash memory and data is written in a flash memory. When time to write data for the time taken to transmit data to a flash memory chip in tT and a flash memory is set to tW, the time taken to write the data for ten sectors in one flash memory chip is 10x (tT+tW).
[0003]The first 528 byte data are written in the k-th flash memory chip among the data of the 528-byte unit which exists ten in interleave, Operation of writing the 528 following byte data in the k+1st flash memory chips, and writing the 3rd 528 byte data in the k-th flash memory again is carried out.
[0004]If it does in this way, a data transfer can be started to the k+1st flash memory chips, without waiting for time until the writing of 528 byte data is completed to the k-th flash memory. Therefore, the time taken to write in the data for ten sectors is 5x(tT+tW)+tT. Compared with the case where it will not interleave if interleave operation is carried out, since it is generally tT<tW, a write time becomes abbreviation half.
[0005]
[Problem to be solved by the invention]However, when interleaved to all the writing operation, there was a problem of lengthening access time as memory storage on the contrary. For example, what is necessary must be just to rewrite 528 bytes of data, when performing operation which rewrites the data of only one sector in memory storage. However, a flash memory writes in in the unit of the block which comprises 528x16=8448 byte. This is based on the following Reasons. A flash memory cannot be overwritten at the data written in now, but writes in by once eliminating data in the unit which is 8448 bytes. In rewriting 528 bytes inside 8448 bytes of a certain block, among 8448 by 528 bytes of that which can be erased and is twisted. After erasing the same address area, 8448 bytes of data which was accepted 528 bytes of 8448 bytes of data stored conventionally, and was changed is written in again, or is written in the area erased [other]. Anyway, 8448 bytes (it is 16 times about 528 bytes) of writing is required. Therefore, in writing in one block, it requires the time of 16x (tT+tW). When rewriting only one sector, or when rewriting the data of two or more sectors, the same time is required for this.
[0006]For example, if the time of 16x(tT+tW)+tT is required if it interleaves when the writing of only two sectors is required, but it does not interleave, writing is completed by 16x (tT+tW). In writing in the sector exceeding 16 on the other hand, the interleaved direction becomes early. To write in 17 sectors, it is necessary to write in 8448 bytes of two blocks. Since it is necessary to rewrite 16 sector data of the 2nd flash memory after rewriting the data of 16 sectors of a one-eyed flash memory if it does not interleave, the time of 2x16x(tT+tW)-tW is required. However, if it interleaves, writing will be made in 16x(tT+tW)+tT.
[0007]It may become late with the case where a write time becomes early, by interleaving as mentioned above.
[0008]
[Means for solving problem]The memory storage of this invention, By two or more flash memory chips and the controller which performs the control. The method which there is a bit to decide and writes in whether the data written in ********** in the memory storage constituted is written in the address with which the flash memory continued, or it writes in two or more flash memories by turns according to the bit is changed.
[0009]
[Mode for carrying out the invention]Drawing 1 is a BURROKU figure of this invention. The address for 101 being a controller and writing the data of CPU which processes a controller, RAM where ROM and CPU which perform the processing program of a controller save data

required for a target temporarily, and a flash memory for the controller 101, It comprises an interface exchanged with the exterior of a data bus and memory storage. 102,103 is a flash memory and is accessed by the controller 101. In this example, although the case where the number of flash memories is two is explained, two or more flash memories may be learned and shoes may be sufficient as them.
[0010]The cylinder from an external interface, a track, It is determined in which area of a actual flash memory data is written with the address mapping table which the controller 101 has in a part of flash memory 102 as the logical address of memory storage called a sector and the information to write in are given to the controller 101.
[0011]This address mapping table is shown in drawing 2. If a cylinder, a track, and a sector are inputted into this address mapping table, the address of the flash memory corresponding to it will be outputted. Data is written in this address. The translation table is defined as every 16 sectors (8448 bytes). The bit which shows whether it interleaves or not is shown in this address mapping table. The controller 101 judges that it is more advantageous whether to interleave with the data volume written in at once, if advantageous, the bit which shows the interleave in a translation table is set, and data is written in ranging over the flash memory 102,103.
[0012]How to write in data is shown in drawing 3. A flash memory writes in data like drawing 3 using the block in the simultaneous position of the flash memory 102,103, although some blocks of 8448 units are included. The turn that the number of drawing 3 writes in data is shown. The 1st data is written in the flash memory 102, and the 2nd data is written in the flash memory 103. Like the following, the data of No. odd is written in the flash memory 102, and the data of No. even is written in the flash memory 103. In reading this data, the bit which shows interleave of an address mapping table is read, and it reads data from the flash memories 102 and 103 by turns. When there is little data volume written in at once, as the bit which shows interleave of an address mapping table is reset and it is shown in drawing 4, data is written in succeeding one flash memory. In reading this data, it reads the data which continued with reference to the bit which shows interleave of an address mapping table.
[0013]
[Effect of the Invention]An access speed can be early carried out by interleaving with the data volume written in at a time as mentioned above judging whether lends and there is, and writing in a flash memory.

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TECHNICAL FIELD

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PRIOR ART

[Description of the Prior Art]When making writing and read-out of the data two or more flash memories with the memory storage constituted by the controller which performs the control, SHINRINDA of a controller, The controller was making the track and the logical address constituted by the sector correspond to the physical address of a flash memory with a translation table. This controller shortened writing time to the flash memory by the method of interleave. Interleave is a method which does not write continuous data in the address with which one flash memory continued, but is written in ranging over two or more memories. For example, to write in the data of ten sectors, since one sector comprises 512 bytes and a total of 528 bytes of 16 bytes of management information of the data, it needs to write 528x10 bytes of data in a flash memory. When writing in a flash memory, after transmitting 528 bytes of data to a flash memory chip and storing in the buffer inside a flash memory, a write command is published to a flash memory and data is written in a flash memory. When time to write data for the time taken to transmit data to a flash memory chip in tT and a flash memory is set to tW, the time taken to write the data for ten sectors in one flash memory chip is 10x (tT+tW).
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EFFECT OF THE INVENTION

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TECHNICAL PROBLEM

[Problem to be solved by the invention]However, when interleaved to all the writing operation, there was a problem of lengthening access time as memory storage on the contrary. For example, what is necessary must be just to rewrite 528 bytes of data, when performing operation which rewrites the data of only one sector in memory storage. However, a flash memory writes in in the unit of the block which comprises 528x16=8448 byte. This is based on the following Reasons. A flash memory cannot be overwritten at the data written in now, but writes in by once eliminating data in the unit which is 8448 bytes. In rewriting 528 bytes inside 8448 bytes of a certain block, among 8448 by 528 bytes of that which can be erased and is twisted. After erasing the same address area, 8448 bytes of data which was accepted 528 bytes of 8448 bytes of data stored conventionally, and was changed is written in again, or is written in the area erased [other]. Anyway, 8448 bytes (it is 16 times about 528 bytes) of writing is required. Therefore, in writing in one block, it requires the time of 16x (tT+tW). When rewriting only one sector, or when rewriting the data of two or more sectors, the same time is required for this.
[0006]For example, if the time of 16x(tT+tW)+tT is required if it interleaves when the writing of only two sectors is required, but it does not interleave, writing is completed by 16x (tT+tW). In writing in the sector exceeding 16 on the other hand, the interleaved direction becomes early. To write in 17 sectors, it is necessary to write in 8448 bytes of two blocks. Since it is necessary to rewrite 16 sector data of the 2nd flash memory after rewriting the data of 16 sectors of a one-eyed flash memory if it does not interleave, the time of 2x16x(tT+tW)-tW is required. However,

if it interleaves, writing will be made in 16x(tT+tW)+tT.
[0007]It may become late with the case where a write time becomes early, by interleaving as mentioned above.

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MEANS

[Means for solving problem]The memory storage of this invention, By two or more flash memory chips and the controller which performs the control. The method which there is a bit to decide and writes in whether the data written in ********** in the memory storage constituted is written in the address with which the flash memory continued, or it writes in two or more flash memories by turns according to the bit is changed.
[0009]
[Mode for carrying out the invention]Drawing 1 is a BURROKU figure of this invention. The address for 101 being a controller and writing the data of CPU which processes a controller, RAM where ROM and CPU which perform the processing program of a controller save data required for a target temporarily, and a flash memory for the controller 101, It comprises an interface exchanged with the exterior of a data bus and memory storage. 102,103 is a flash memory and is accessed by the controller 101. In this example, although the case where the number of flash memories is two is explained, two or more flash memories may be learned and shoes may be sufficient as them.
[0010]The cylinder from an external interface, a track, It is determined in which area of a actual flash memory data is written with the address mapping table which the controller 101 has in a part of flash memory 102 as the logical address of memory storage called a sector and the information to write in are given to the controller 101.
[0011]This address mapping table is shown in drawing 2. If a cylinder, a track, and a sector are inputted into this address mapping table, the address of the flash memory corresponding to it will be outputted. Data is written in this address. The translation table is defined as every 16 sectors (8448 bytes). The bit which shows whether it interleaves or not is shown in this address mapping table. The controller 101 judges that it is more advantageous whether to interleave with the data volume written in at once, if advantageous, the bit which shows the interleave in a translation table is set, and data is written in ranging over the flash memory 102,103.
[0012]How to write in data is shown in drawing 3. A flash memory writes in data like drawing 3 using the block in the simultaneous position of the flash memory 102,103, although some blocks of 8448 units are included. The turn that the number of drawing 3 writes in data is shown. The

1st data is written in the flash memory 102, and the 2nd data is written in the flash memory 103. Like the following, the data of No. odd is written in the flash memory 102, and the data of No. even is written in the flash memory 103. In reading this data, the bit which shows interleave of an address mapping table is read, and it reads data from the flash memories 102 and 103 by turns. When there is little data volume written in at once, as the bit which shows interleave of an address mapping table is reset and it is shown in drawing 4, data is written in succeeding one flash memory. In reading this data, it reads the data which continued with reference to the bit which shows interleave of an address mapping table.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]The system configuration figure showing 1 embodiment of this invention.
[Drawing 2]The figure of an address mapping table.
[Drawing 3]The figure of the example of data writing at the time of interleaving.
[Drawing 4]The figure of the example of data writing when not interleaving.
[Explanations of letters or numerals]
101 Controller
102 Flash memory
103 Flash memory

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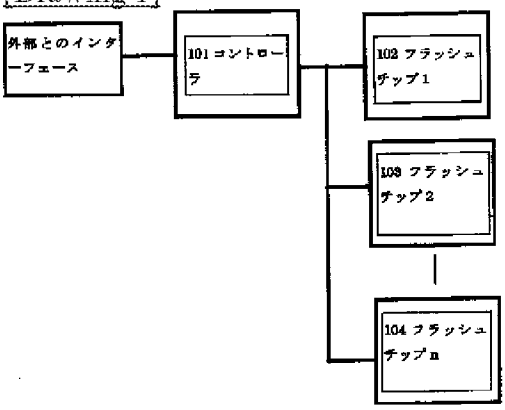
DRAWINGS

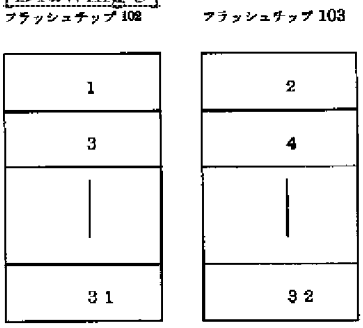
[Drawing 1]



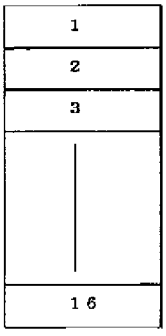
[Drawing 2]

シリンダ/トラック/セクタ	アドレス	インターリーブ
0/0/1～16	ブロックの先頭アドレス	y/n
0/0/17～31	ブロックの先頭アドレス	y/n
1/n/n～n+15	ブロックの先頭アドレス	y/n

[Drawing 3]



[Drawing 4]



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